**IN THE SPECIFICATION**

**Please amend the paragraph beginning at page 7, line 21 as follows:**

Fig. 18 is a plane view showing the layout of pads and input and output cells for several modifications;

**Please insert the following paragraphs following page 7, line 23:**

Fig. 20 is a cross-sectional view of the flip-chip semiconductor device of Fig. 3; and

Fig. 21 is a plane view showing a portion of a layout of a flip-chip semiconductor device consistent with the principles of the device of Fig. 3.

**Please amend the paragraph beginning at page 8, line 13 as follows:**

Most of the peripheral area 1b is assigned to input and output circuits such as those labeled with 21/ 22/ 23 and signal pads such as those labeled with 31/ 32/ 33. The input and output cells are herein below referred to as "input and output cells", and the signal pads are electrically connected to the input and output cells. Each of the input and output cells is implemented by an output driver circuit and/ or input buffer circuit. An input and output controlling circuit may be further incorporated in the input and output cell. An input and output control circuit may be further incorporated in the input and output cell. Although the input and output cells are drawn on a level with the signal pads in figures 3 and 4, the flip chip semiconductor device has a multi- layered structure, and the input and output cells are assigned a certain level lower than the level assigned to the signal pads. This assigned level may be referred to as a "cell forming layer." The signal pads are formed on the highest level of the multi- layered structure. The highest level is

herein below referred to as "pad forming layer". Figure 20 presents a cross-sectional view through the flip-chip semiconductor device 1 of Figure 3, illustrating cell forming layer 1e, pad forming layer 1g, and intermediate layers 1f.

**Please amend the paragraph beginning at page 11, line 21 as follows:**

The inner area of the pad forming layer is assigned to power supply pads 13/ 14. The power supply pads 13 are assigned to the power voltage VDD, and the power supply pads 14 are assigned to the other power voltage VSS. The power supply pads 13 are represented by small squares in figure 3, and each of the power supply pads 13 is hatched with oblique lines drawn from the upper corner of the left side to the lower corner of the right side. The power supply pads 14 are also represented by small squares. However, each of the power supply pads 14 is hatched with oblique lines drawn from the upper corner of the right side to the lower corner of the left side. Thus, the potential level on the power supply pads 13/ 14 is discriminated by comparing the direction of the hatching lines. As will be seen in figure 3, the power supply pads 13 are arranged in staggered fashion. On the other hand, the other power supply pads 14 occupy the vacant areas among the power supply pads 13, and are also laid on a staggered pattern. Macro-cells such as logic cells are fabricated under the inner area on the pad forming layer, and the power voltages VSS and VDD are supplied from the power supply pads 13/ 14 to the logic cells through via-holes. However, the input and output cells do not perfectly occupy the peripheral area 1b of the certain level. In other words, there are vacancies among the regions assigned to the input and output cells in the peripheral area 1b on the